## **MiD** 2019

August 27 - 30, 2019 / HICO, Gyeongju, Korea



Company Name	SILVACO	Company Logo
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Company Introduction	Silvaco, Inc. is a leading EDA provider of software tools used for process and device development and for analog/mixed-signal, power IC and memory design. The portfolio also includes tools for power integrity sign off, reduction of extracted netlist, variation analysis and also production-proven intellectual property (IP) cores. Silvaco delivers a full TCAD-to-Signoff flow for vertical markets including: displays, power electronics, optical devices, radiation & soft error reliability, analog and HSIO design, library and memory design, advanced CMOS process and IP development. The company is headquartered in Santa Clara, California, and has a global presence with offices located in North America, Europe, Japan and Asia. For over 30 years, Silvaco has enabled customers to bring superior products to market in the shortest time with reduced cost. Semiconductor fabs and design houses from around the globe have relied on Silvaco's expertise to help develop the "technology behind the chip". Silvaco's mission is to help our customers accelerate the pace of technological innovation and their time to market while reducing their costs in developing the next-generation chips. We strive to understand our customers' challenges to tailor the innovative products, services and support they need to succeed in their technology development and productivity goals.	

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	Power integrity signoff from block (analog, SRAM, custom digital) to full chip level including power,	
	EM/IR and thermal analysis- InVar	
	Full custom design flow including schematic entry, layout, simulation and verification	
	Large portfolio of PDKs across many foundries with emphasis on AMS, HV, BCD and CIS processes	
	16nm and 10nm FinFET ready Parallel SPICE simulator being extended to support FastSPICE	
	applications	
	Variation-aware design tools comprising of Fast Monte Carlo, Local mismatch, statistical corners, high	
	sigma analysis and statistical verification of standard cell libraries	
	• Extracted netlist analysis & reduction tools providing parasitic reduction, design analysis & verification,	
Exhibit	comparison of extracted netlists including parasitics	
Description	Automated standard Cell & SRAM characterization environment	
	3D parasitic RC extractor used for detailed and accurate FinFET SRAM extraction	
	SPICE modeling for large set of model types including HiSIM_HV for power devices and UOTFT for	
	organic and oxide TFTs	
	Pixel and interconnect RC extraction for TFT displays	
	3D TCAD products used for large application space, including rapid FinFET prototyping, large structure	
	parallelized simulations for multi-cell IGBTs, robust, stable oxidation simulation for trench MOS power	
	devices and CMOS image sensors, high precision SiC/GaN simulation, advanced etch for 3D NAND Flash	
	and STT MRAM, SEE and total dose reliability simulation	
	• Victory™ for 2D and 3D TCAD process and device simulation of nanometer CMOS, power devices,	
	automotive applications and atomistic simulation of nano-meter scale devices such as quantum dots	
	• Clever LCD™ Clever LCD, a 3D simulator calculating liquid crystal (LC) director by a finite element field	
	solver for display applications	
	• Gateway™, Expert™, Guardian™ for schematic driven physical layout with scripting and native DRC/LVS	
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