Anomalous Increase of Field-Effect Mobility in In-Ga-Zn-O Thin-Film Transistors Caused by Dry-Etching Damage Through Etching-Stopper

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In-Ga-Zn-O (IGZO) thin-film transistors (TFTs) have been received great attention for use in next-generation active-matrix displays because it exhibits higher electron mobility ($\mu > 10 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$) as compared with conventional amorphous Si TFTs [1]. Bottom-gate structure with an etching-stopper (ES) is widely utilized for the IGZO TFTs. In this research, we report the influence of plasma induced damage during dry-etching (D/E) of source/drain (S/D) electrodes on field effect mobility ($\mu$) of the IGZO TFTs.

The detail fabrication process of the IGZO TFTs was reported elsewhere [2]. The thickness of SiO$_x$-ES layer, which was deposited by plasma-enhanced chemical vapor deposition (PE-CVD), was varied from 100 to 200 nm to change the channel protection ability against the S/D-D/E process. The indium-tin-oxide (ITO) as S/D electrodes were patterned by D/E or wet etching (W/E). For the D/E, an inductively coupled plasma etching was used in a mixed gas of CH$_4$/Ar with substrate bias of 60 W. Finally, the TFTs were post-annealed in N$_2$ at 250 °C for 1 hour.

Fig. 1 shows the transfer characteristics of the IGZO TFTs with (a) ES:100nm+S/D-W/E, (b) ES:100nm+S/D-D/E and (c) ES:200nm+S/D-D/E. The channel width and length (W/L) of Fig. 1 were 50/20 (µm). When the ES thickness was 200 nm, the $\mu$ of S/D-D/E TFT was almost same as the TFT with S/D-W/E. However, $\mu$ of the S/D-D/E TFT increased to around 30 cm$^2$V$^{-1}$s$^{-1}$ when the ES thickness reduced to be 100 nm. This result suggests that the S/D-D/E induced damage caused an anomalous increase of the $\mu$ of the TFT when the ES thickness reduced. Fig. 2 shows the results of transfer length method (TLM) obtain from those TFTs. For the TFTs with ES:200nm+S/D-D/E and ES:100nm+S/D-W/E as shown in Fig. 2-(a) and (c), L dependence and intersection of the resistances are clearly obtained from the slopes at different gate voltages. However, the TFT with ES:100nm+S/D-D/E, which observed an anomalous increase of $\mu$, was not able to identify the channel length dependence as shown in Fig. 2(b). These results suggest that plasma induced damage into the IGZO channel through thinner ES-layer, and it influenced on the channel resistance, result in an overestimation of $\mu$.

The detailed mechanisms for the anomalous increase of $\mu$ will be presented at the conference.

![Graph 1](image1.png)

**Fig. 1.** Transfer characteristics of the IGZO TFTs with (a) ES:100nm+S/D-W/E, (b) ES:100nm+S/D-D/E, and (c) ES:200nm+S/D-D/E

![Graph 2](image2.png)

**Fig. 2.** TLM results of the TFT with (a) ES:100nm+S/D-W/E, (b) ES:100nm+S/D-D/E, and (c) ES:200nm+S/D-D/E

**References**


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