

Session 11

11. TFT Circuits

Wednesday, October 12, 2011 / 13:30 ~ 14:50

Room 305

Chairs: Reiji Hattori (ASTEC, Japan)

Bong Hyun You (Seoul National Univ., Korea)

-
- | | | |
|----------------------|-------------|---|
| 13:30 ~ 13:50 | 11-1 | A Novel Amorphous Silicon TFT Gate Driver Circuit with Optimized Design for Integrated Display Panel Manufacturing
<i>Po-Jui Lin, I-Hsiu Lo, Yiming Li, and Cheng-Han Shen (Nat'l Chiao Tung Univ., Taiwan)</i> |
|
 | | |
| 13:50 ~ 14:10 | 11-2 | N-Channel TFT Logic Gates with Full Output Voltage Swing
<i>Tao Ren, HongKyun Leem, Jisun Kim, YounKyung Kim, JoonDong Kim, HwanSool Oh (Konkuk Univ., Korea), JaeEun Pi, Shinhyuk Yang, Min Ki Ryu, Sang-Hee Ko Park, Byounggon Yu (ETRI, Korea), KeeChan Park (Konkuk Univ., Korea)</i> |
|
 | | |
| 14:10 ~ 14:30 | 11-3 | Design for Less Stress in the Pull-Down Transistors for On-panel TFT Gate Drivers
<i>Nan Xiong Huang, Miin Shyue Shiau, Po Hung Chen, Hong-Chong Wu, Heng-Shou Hsu, and Don Gey Liu (Feng Chia Univ., Taiwan)</i> |
|
 | | |
| 14:30 ~ 14:50 | 11-4 | Low Power Consumption Shift Register Using Depletion Mode Amorphous In-Ga-Zn-O TFTs
<i>Seung-Jin Yoo, Jin-Seong Kang, and Oh-Kyong Kwon (Hanyang Univ., Korea)</i> |